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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/816,269 | 03/31/2004 | Robert P. Masleid | TRAN-P293 | 9824 |

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| EXAMINER | |
|---|---|
| PHAM, LONG | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/816,269 | MASLEID ET AL. | |
| | Examiner | Art Unit | |
| | Long Pham | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) 3-5,13-15 and 23-25 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,6-12,16-22 and 26-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of claims 1-2, 6-12, 16-22, and 26-33 in the reply filed on 09/16/95 is acknowledged.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 6-12, 16-22, and 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pelham et al. (US patent 6,936,898) in combination with Takahashi et al. (US publication 2001/0024859).

With respect to claim 1, Pelham et al. '898 teach a semiconductor device having a surface, comprising (see figs. 1, 2, 3A-3B, 4, and 5 and associated text, particularly fig. 4):

A plurality of conductive sub-surface regions 412A, 412B, 412C, 410A, and 410B of a first conductivity (N) each formed beneath said surface, wherein said conductive sub-surface regions form a sub-surface structure for routing a body-bias voltage, wherein said sub-surface structure has a perimeter; and

An isolation structure 440A,440B formed within said perimeter of said sub-surface structure such that said isolation structure creates a gap in said sub-surface structure.

Pelham et al. '898 fail to teach forming a metal interconnect over the sub-surface regions.

Takahashi et al. teach forming a metal structure or silicide layer over semiconductor regions to improve the operation speed of the device.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Takahashi et al. into the device of Pelham et al. to attain the above benefit.

Further with respect to claim 11, Takahashi et al. teach coupling the metal structure to the semiconductor regions but fail to teach the coupling is done via contacts.

However, the coupling of metal to semiconductor regions via contacts is well-known.

With respect to claim 2, Pelham et al. further teach that the sub-surface structure is a diagonal sub-surface mesh structure. See fig. 4 and col. 4, lines 30-50.

With respect to claim 6, Pelham et al. further teach that each conductive sub-surface region has an N-type doping. See claim 2.

With respect to claim 7, Pelham et al. further teach that the sub-surface region has a P-type doping. See claim 6.

With respect to claim 8, Pelham et al. further teach that the sub-surface region has a strip shape. See claim 9.

With respect to claim 9, Takahashi et al. teach metal structure or silicide has layer shape but fail to teach that the metal structure is made of wire shape.

However, the use of wire shaped metal structure for connecting semiconductor elements or regions is well-known.

With respect to claim 10, Pelham et al. further teach a plurality of second conductive sub-surface regions 412A, 412B, 412C, 410A, and 410B of the first conductivity wherein each second conductive sub-surface region has a continuous sub-surface layer shape. See figs. 4 and 5 and associated text.

With respect to claims 11 and 20, Pelham et al. '898 teach a semiconductor device having a surface, comprising (see figs. 1, 2, 3A-3B, 4, and 5 and associated text, particularly fig. 4):

A plurality of conductive sub-surface regions 412A, 412B, 412C, 410A, and 410B of a first conductivity each formed beneath said surface, wherein said first plurality of conductive sub-surface regions form a first sub-surface structure for routing a body-bias voltage;

A plurality of conductive sub-surface regions 412A, 412B, 412C, 410A, and 410B of said first conductivity type each formed beneath said surface, wherein said second plurality of conductive sub-surface regions form a second sub-surface structure for routing said body-bias voltage; and

An isolation structure 440A,440B formed between said first and said sub-surface structures such that said isolation structure creates a gap between said first sub-surface structure and said second sub-surface structure.

Pelham et al. '898 fail to teach forming a metal structure or metal interconnect over the sub-surface regions.

Takahashi et al. teach forming a metal structure or silicide layer over semiconductor regions to improve the operation speed of the device.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Takahashi et al. into the device of Pelham et al. to attain the above benefit.

Further with respect to claim 1, Takahashi et al. teach coupling the metal structure to the semiconductor regions but fail to teach the coupling is done via contacts.

However, the coupling of metal to semiconductor regions via contacts is well-known.

With respect to claim 12, Pelham et al. further teach that the first sub-surface structure is a first diagonal sub-surface mesh structure and the second sub-

surface structure is a second diagonal sub-surface mesh structure. See fig. 4 and col. 4, lines 30-50.

With respect to claim 16, Pelham et al. further teach that each conductive sub-surface region has an N-type doping. See claim 2.

With respect to claim 17, Pelham et al. further teach that the sub-surface region has a P-type doping. See claim 6.

With respect to claim 18, Pelham et al. further teach that the sub-surface region has a strip shape. See claim 9.

With respect to claim 19, Takahashi et al. teach metal structure or silicide has layer shape but fail to teach that the metal structure is made of wire shape.

However, the use of wire shaped metal structure for connecting semiconductor elements or regions is well-known.

With respect to claim 20, Pelham et al. further teach that each second conductive sub-surface region has a continuous sub-surface layer shape. See figs. 1, 2, 3A-3B, 4, and 5 and associated text, particularly fig. 4.

With respect to claim 21, Pelham et al. '898 teach a semiconductor device having a surface, comprising (see figs. 1, 2, 3A-3B, 4, and 5 and associated text, particularly fig. 4):

A plurality of conductive sub-surface regions 412A, 412B, 412C, 410A, and 410B of a first conductivity each formed beneath said surface, wherein said conductive sub-surface regions form a sub-surface structure for routing a body-bias voltage, wherein said sub-surface structure has a perimeter; and

An isolation structure formed within said perimeter of said sub-surface structure such that said isolation structure creates a gap in said sub-surface structure.

Pelham et al. '898 fail to teach forming a metal interconnect over the sub-surface regions.

Takahashi et al. teach forming a metal structure or silicide layer over semiconductor regions to improve the operation speed of the device.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Takahashi et al. into the device of Pelham et al. to attain the above benefit.

With respect to claim 22, Pelham et al. further teach that the sub-surface structure is a diagonal sub-surface mesh structure. See fig. 4 and col. 4, lines 30-50.

With respect to claim 26, Pelham et al. further teach that each conductive sub-surface region has an N-type doping. See claim 2.

With respect to claim 27, Pelham et al. further teach that the sub-surface region has a P-type doping. See claim 6.

With respect to claim 28, Pelham et al. further teach that the sub-surface region has a strip shape. See claim 9.

With respect to claims 29, 30, and 31, Takahashi et al. teach metal structure or silicide has layer shape but fail to teach that the metal structure is made of wire shape.

However, the use of wire shaped metal structure for connecting semiconductor elements or regions is well-known.

Further with respect to claims 29, 30, and 31, the use of polysilicon, diffusion, and silicide wires as connecting structures is well-known.

With respect to claim 32, Pelham et al. further teach that each second conductive sub-surface region has a continuous sub-surface layer shape. See figs. 1, 2, 3A-3B, 4, and 5 and associated text, particularly fig. 4.

With respect to claim 33, Pelham et al. further teach that the isolation structure divides said sub-surface structure into a first portion and a second portion. See figs. 1, 2, 3A-3B, 4, and 5 and associated text, particularly fig. 4.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP